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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,269	04/05/2005	William A Steer	GB 020172	4629

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P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
CHOWDHURY, AFROZA Y	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/530,269	STEER, WILLIAM A	
	Examiner	Art Unit	
	AFROZA Y. CHOWDHURY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-15* is/are rejected.

7)☒ Claim(s) *5-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment received on **April 29, 2009** has been entered. Claims 1-15 are pending. Applicant's arguments are addressed herein below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Oomura** (US Pub. 2003/0020413) in view of **Pae et al.** (EP1221686).

As to claim 12, Oomura discloses a method of addressing an active matrix electroluminescent display device comprising, an array of display pixels (fig. 2),

in which each pixel comprises an electroluminescent (EL) display element (fig. 6(OLED)) and a drive transistor (fig. 6(T1)) for driving a current ([0088]) through the display element (fig. 6(OLED)), the method comprising, for each pixel:

applying a voltage (fig. 6) to the drive transistor (fig. 6(T1)) to drive a current through the display element (fig. 6(OLED), [0088], [0093], [0102]), the current being drawn from a current-measurement supply line (fig. 6, [0102]),

processing the current using feedback control circuitry outside the array of pixels (fig. 6) and having an input representing the desired current ([0091] – [0093]),

generating a control voltage in the feedback control circuitry for the drive transistor (fig. 6(T2)) using the processed current (fig. 6, [0102]),

within the pixel, storing a voltage (fig. 6, C) derived from the control voltage (abstract, [0094], [0102]); and

drawing current from a power supply line (fig. 6(Vdd)) to illuminate the display element (fig. 6(OLED)).

Oomura does not teach implementing a feedback control loop which reaches equilibrium when the current corresponds to the desired current.

Pae et al. teaches implementing a feedback control loop (fig. 2, 3, col. 5, [0035], [0040]) which reaches equilibrium [0041] when the current corresponds to the desired current,

supplying the control voltage (col. 5, [0034], [0040]) to the pixel; and

applying the stored voltage (fig. 2, col. 5, [0034]) to the gate of the drive transistor (fig. 2(P0)).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to combine the driving circuit of Pae et al. with Oomura's active matrix display to make an electroluminescent display device in order to drive current for realizing a desired luminance.

As to claim 13, Oomura (as modified by Pae et al.) teaches a method wherein a processing the current comprises converting the current into a voltage (fig. 3, col. 6, [0045], in Pae et al), and comparing the voltage (fig. 3, col. 6, [0045], in Pae et al.) with an input voltage representing the desired current to produce an amplified differential output (col. 6, [0042], in Pae et al.).

As to claim 14, Oomura (as modified by Pae et al.) teaches a method where the control voltage comprises the amplified differential output (col. 6 in Oomura).

4. Claims 1-4, 8-11, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Oomura** (US Pub. 2003/0020413) in view of **Miyazawa** (US Pub. 2004/0036664).

As to claim 1, Oomura discloses an active matrix display comprising:

an electroluminescent (EL) display element (fig. 6(OLED)) and

a drive transistor (fig. 6(T1)) for driving a current ([0088]) through the display element (fig. 6(OLED));

a first switch (fig. 6(T2)) enabling power from a power supply line (fig. 6(Vdd)) to be supplied to the display element ([0088], [0091]),

a second switch (fig. (T5)) for routing current from a current-measurement supply line (fig. 6(Im)) to the display element (fig. 6(OLED), [0088], [0093], [0102]),

a control line (fig. 6(Vw)) for controlling the gate voltage applied to the drive transistor (fig. 6(T1)), and

a driving circuit where a feedback system is provided between the current-measurement supply line (fig. 6(Im)) and the control line (fig. 6(Vm), [0102]).

Oomura does not teach that the first and second switches being operated in complementary manner.

Miyazawa teaches a first and second switches being operated in complementary manner ([0112]).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to modify Oomura's display device using Miyazawa's idea of designing a driving circuit where a first and second switches being operated in complementary manner to make an active matrix electroluminescent display with desired luminescence of the pixels.

As to claim 2, Oomura (as modified by Miyazawa) teaches a device where the feedback system enables a gate voltage to be determined corresponding to a desired current flow through the drive transistor (fig. 6, in Oomura).

As to claim 3, Oomura (as modified by Miyazawa) teaches a device wherein the feedback system is provided in a column driver of the display device (fig. 6, in Oomura).

As to claim 4, Oomura (as modified by Miyazawa) teaches a device where each pixel further comprises a storage capacitor (fig. 6,C in Oomura) for storing a gate-source voltage of the driving transistor (abstract, [0094], [0102], in Oomura).

As to claim 8, Oomura (as modified by Miyazawa) teaches a device wherein each switch comprises a transistor (fig. 6(T2, T5), in Oomura).

As to claim 9, Oomura (as modified by Miyazawa) teaches a device wherein one of the switches is an NMOS TFT and the other is a PMOS TFT ([0112], in Miyazawa).

As to claim 10, Oomura (as modified by Miyazawa) teaches a device as claimed in any preceding claim, wherein the feedback system comprises:

a current-to-voltage converter section for providing a first voltage corresponding to the current drawn from the current-measurement supply line (fig. 6, [0102], in Oomura);

a comparator section for comparing the first voltage with an input voltage representing the desired current ([0102], in Oomura); and

a drive section for providing a voltage on the control line (0088], in Oomura), the feedback loop being in equilibrium when the control line voltage provides drive of the drive transistor giving rise to a current corresponding to the input voltage ([0092], in Oomura).

As to claim 11, Oomura (as modified by Miyazawa) teaches a device as claimed in any preceding claim, wherein the device is operable in two modes:

a first mode in which a desired pixel drive current is drawn from the current-measurement supply line and the feedback system generates the corresponding gate voltage for the drive transistor (fig. 6, in Oomura), the corresponding gate-source voltage for the drive transistor being stored (fig. 6, [0094], in Oomura); and

a second mode in which a current is driven through the drive transistor (fig. 6, in Oomura) and the EL display element using the stored gate-source voltage ([0088], in Oomura).

As to claim 15, Oomura (as modified by Miyazawa) teaches a method wherein current is drawn from the power supply line through a first switch (fig. 6(T2), in Oomura) and

current is drawn from the current-measurement supply line (fig. 6(Im), in Oomura) through a second switch (fig. 6(T5), in Oomura),

the first switch (fig. 6(T2), in Oomura) being used after an initial pixel programming phase ([0093], in Oomura),

the second switch (fig. 6(T5), in Oomura) being used during the initial pixel programming phase ([0093] - [0093], in Oomura), and

the first and second switches being operated in complimentary manner ([0112], in Miyazawa).

Allowable Subject Matter

5. Claims 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claim 5, prior art does not show, **"an address transistor connected between the control line and the gate of the drive transistor"** in combination with other limitations of claim 5.

As to claim 6, prior art does not show, **"address transistor, and the first and second switches are each controlled by a shared control line"** in combination with other limitations of claim 6.

As to claim 7, prior art does not show, **"the address transistor and the second switch are controlled synchronously"** in combination with other limitations of claim 7.

Response to Arguments

6. Applicant's arguments filed **April 29, 2009** have been fully considered but they are not persuasive.

On page 2 of Remarks, lines 3-5, Applicant asserts, **"There is no description or suggestion of applying a voltage to the drive transistor to drive a current through the display element, the current being drawn from a current-measurement supply**

line ... in claim 12." The Examiner respectfully disagrees to this assertion. Oomura clearly teaches applying a voltage to the drive transistor (fig. 6(T1)) to drive a current through the display element (fig. 6(OLED), the current being drawn from a current-measurement supply line (fig. 6, [0088], [0093], [0102]).

On page 3 of Remarks, 2nd paragraph, Applicant states that **Oomura does not suggest a second switch for routing current from a current-measurement supply line to the display element.** The Examiner again respectfully disagrees to this statement. Oomura discloses a second switch (fig. (T5)) for routing current from a current-measurement supply line (fig. 6(Im)) to the display element (fig. 6(OLED), [0088], [0093], [0102]).

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AFROZA Y. CHOWDHURY whose telephone number is (571)270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC
7/28/2009

/Bipin Shalwala/
Supervisory Patent Examiner, Art Unit 2629